

**TTO NITRIDE LINER FOR IMPROVED  
COLLAR PROTECTION AND TTO RELIABILITY**

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**ABSTRACT OF THE DISCLOSURE**

A structure and method which enables the deposit of a thin nitride liner just before  
10 Trench Top Oxide TTO (High Density Plasma) HDP deposition during the formation of a vertical MOSFET DRAM cell device. This liner is subsequently removed after TTO sidewall etch. One function of this liner is to protect the collar oxide from being etched during the TTO oxide sidewall etch and generally provides lateral etch protection which is not realized in the current processing scheme. The process sequence does not rely on  
15 previously deposited films for collar protection, and decouples TTO sidewall etch protection from previous processing steps to provide additional process flexibility, such as allowing a thinner strap Cut Mask nitride and greater nitride etching during node nitride removal and buried strap nitrided interface removal. Advantageously, the presence of the nitride liner beneath the TTO reduces possibility of TTO dielectric  
20 breakdown between the gate and capacitor node electrode of the vertical MOSFET DRAM cell, while assuring strap diffusion to gate conductor overlap.